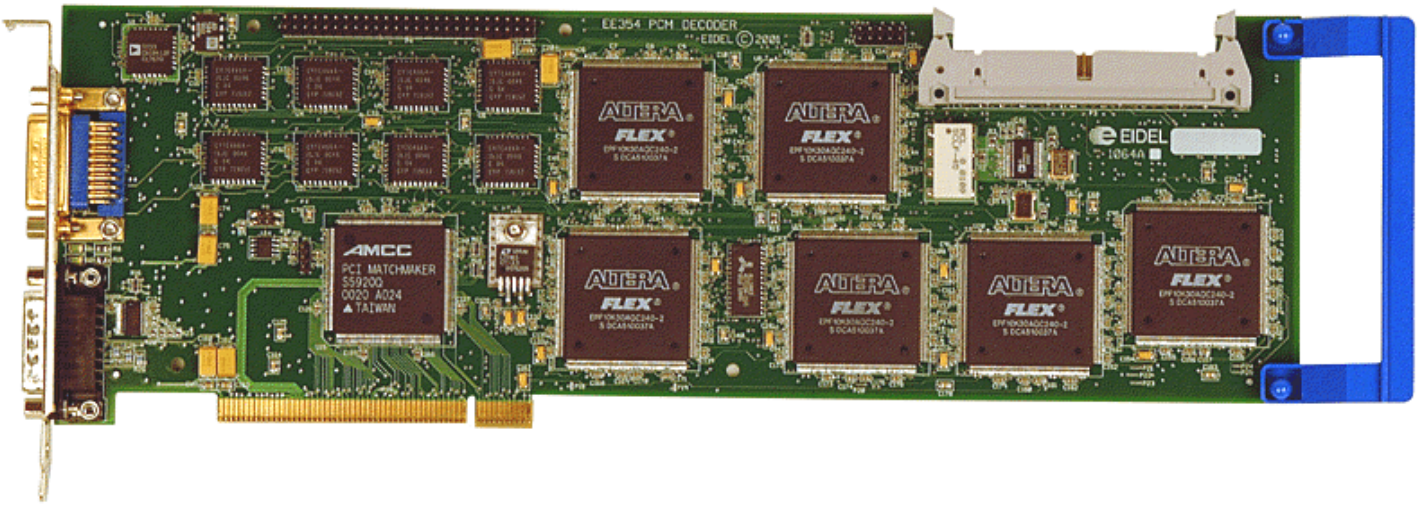


EE 350 TELEMETRY DECODER

EE 354 Decoder, PCI board



The EE350 Telemetry Decoder System covers the IRIG 106-01 PCM standard class I - II and Arinc 573. Asynchronous embedded packets decoding is included. EE350 is based on 40 years of PCM decoder experience at Eidel.

The EE350 system consists of plug-in cards for the common PC 32 bit PCI bus and Windows System Software. All functions from the raw bitstream to presentation, data storage and analysis are covered.

EE350 is an open system, allowing the User to implement individual requirements. The EE351 DLL is the interface level for both User designed and EE352 application software.

EE354 Decoder

- Complete Decoder on one PCI-bus card.
- Frame & Format Synchronizer to 18 Mbps.
- High speed PCM data storage to disk.
- Time tagging of Data with 1 μ s resolution.
- Analog & Digital selected signal outputs.
- PCM Simulator, 0-20 Mbps. All words programmable or from data file.
- IRIG-B Time Code Reader.

EE355 Bitsync

- Bitsynchronizer for all IRIG-106 codes up to 20 Mbps (NRZ). Piggyback to EE354.
- Analog, digital and RS422 type data inputs.

EE356 Bitsync

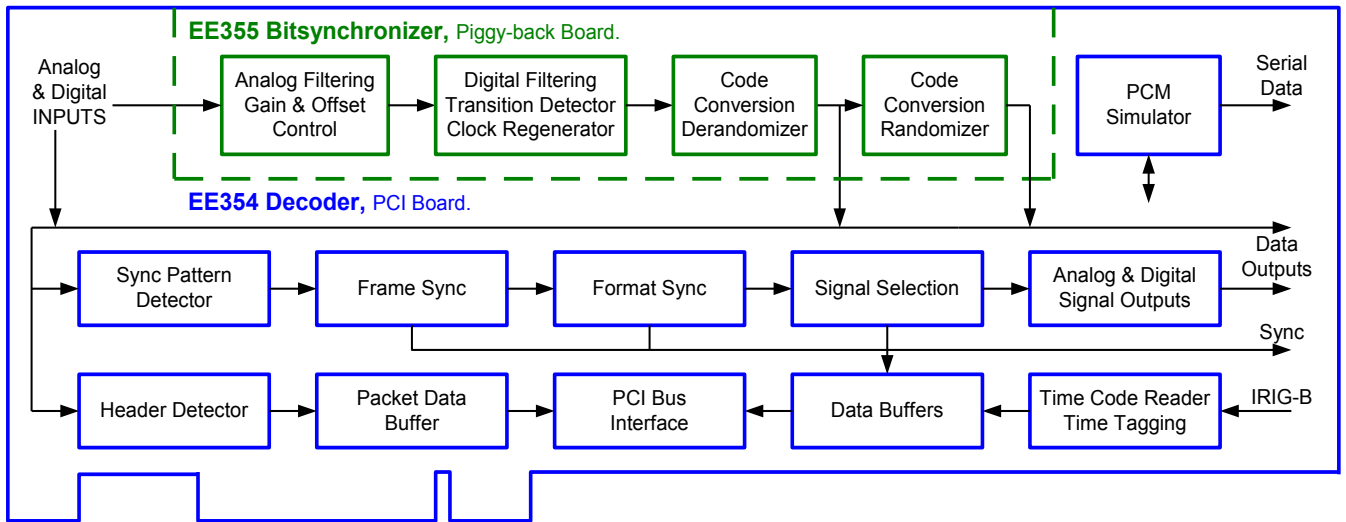
- EE355 card in a standalone box with power.
- Online controlled by the EE352 software or standalone with 8 preprogrammed formats.

EE351 Driver

- 32 bit DLL contains all interfaces between hardware and software.
- Available for User designed applications.

EE352 Software

- Complete System Software for Windows NT 4.0, 2000 and XP Professional.
- Configuration menus for data input structure and hardware setup.
- Data displays for Numeric, Bargraph and Graphic traces.
- Signal scaling to physical parameter.
- Data stream storage controlled by time, limit check or external event.
- Playback of stored data to displays.
- Export of scaled data to ASCII files.
- Short learning time, ease of use.



EE350 Decoder System.

A complete synchronizer for one bitstream is included on the **EE354**, a full size PCI-bus board. It covers frame/format synchronisation, signal selection and data routing towards the output interfaces. Serial data and bitclock are received from the EE355 bitsync or from an external source.

The **EE355** Bitsync has an analog frontend with AGC and filtering. Signal conditioning and bitsynchronisation are done in the digital domain.

EE356 is a standalone bitsynchroniser including the EE355 board. EE356 can be preloaded with 8 independent PCM definitions or operate online with the EE352 software.

The **EE351** DLL contains all interfaces between the hardware and the decoder application software.

The **EE352** Decoder system software includes all setup menus, user interfaces and presentations.

EE354 Specifications.

Inputs, NRZ-L + CP:

External RS422 or TTL. 10k Ω .
Internal Simulator.
Internal piggyback Bitsync.

Inputs, Status, Events:

Lock status of external bitsync. Polarity selection.
Data recording trigger.

Bitrate: 0 to 18 Mbps

Wordlength:

4 to 16 Databit plus odd, even or no parity.
Variable Wordlength.

Alignment: MSB first. LSB first per signal by software.

Frاملength:

3 to 8192 Words inclusive Frame Sync Pattern.

Formatlength: 1 to 1024 Frames. 3 to 524288 Words.

Frame Sync, IRIG 106:

4 to 64 bit, maskable.
Error threshold: 0-7. Aperture: ± 0 to ± 3 .

Frame Sync, ARINC 573:

4 standard patterns of frame 1-4, LSB or MSB first.
Error threshold: 0-7. Aperture: ± 0 to ± 3 .

Format Sync:

- A: Frame counter, counting from 0 and up.
- B: Frame Recycle Code. Unique selectable bit pattern. Any bits maskable. Error threshold: 0-1.
- C: Arinc 573 use separate frame sync patterns to identify each of the four frames.

Embedded Data:

Synchronous and asynchronous embedded frames (packets) of IRIG class I structure, maximum 3. Located in any selected word(s) of the frame.

Packet Data:

Asynchronous data packets, max 3 decoded at one time.

Header: 4 to 32 bit, maskable. Error threshold: 0-1.

Length: 1 to 65536 words.

Fixed wordlength 4-16 bit per packet.

Data Storage:

All words are stored to disk. The stored data is time stamped each frame with a resolution of 1 μ s. Time is synchronised from the IRIG-B reader or other time source in the PC.

Data Buffers:

1023 selectable signals are in a real time updated to a DPRAM, readable by the PC.

4 large FIFOs are used to capture data from selected signals for special processing, packets and recording.

Analog Outputs:

4 DACs of 12 bit resolution, scale 0 to +5V. Data is from real-time, software processed or playback.

Digital Outputs:

2 ports of 16 bit parallel with strobe signal. Data is from real-time, software processed or playback.

Control Outputs:

CP, WP, SFP, LOCK.

Time Code Reader.

Input: IRIG B serial time code, 1 kHz carrier, 1 to 10 Vp-p.

PCM Simulator.

PCM Format:

Any continuous structure related to IRIG-106 class I/II and to Arinc 573. Software generated.

Data Contents:

Menu programmed values or sequences for any selected signal or word/frame positions.
Playback of decoder recorded data file, or any type file.

Bitrate:

10 to 25 Mbps. 0.1 Hz resolution.

Output Codes:

NRZ-L, M, S; RNRZ-L (11, 13, 15 or 17 forward);
BiPhase-L, M, S; Miller-M, S.

Output Signals:

Selected Code, Differential, TTL levels.
NRZ-L, CP, trigger, TTL level.

Subject to change without further notice.

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